REMARKS

Two paragraphs of the specification have been amended to conform the specification to the filed drawings. In particular, the reference number 56 in FIG. 2 of analog display signals has been inserted into the specification.

A spelling error has been corrected in claim 6.

Claims 3 and 4 have been amended to be in independent form. Claims 1-13 remain in the application.

The Examiner allowed claims 6-13 and stated that claims 3 and 4 would be allowable if rewritten in independent form including all limitations of base and intervening claims.

Accordingly, claim 3 has been rewritten in independent form including the limitations of claim 1 and claim 4 has been rewritten in independent form including the limitations of claim 1.

The Examiner rejected claim 1 under 35 USC §103(a) as being unpatentable over Eglit (5,796,392).

As recited in its preamble, Applicant's independent claim 1 is directed to "a method of generating a digital display signal from an analog signal that is limited to 2^N discrete analog levels". This is a situation which occurs, for example, when a computer element (e.g., PC graphics card 20 in Applicant's FIG. 1) uses a set of digital-to-analog converters (e.g., DACs 26 in Applicant's FIG. 1) to provide cathode ray tube (CRT) analog display signals (e.g., signals 56 in Applicant's FIG. 2).

In a first process step of claim 1, these analog signals are sampled in response to a sample clock to provide analog samples. The provided samples are then quantized in a second process step to provide an M-bit digital display signal wherein M exceeds N. In a final process step, at least one of the frequency and phase of the sample clock is adjusted to substantially restrict the codes of the M-bit digital display signal to 2^N different codes.

The quantizing step of claim 1 is particularly important because it provides the enhanced resolution of the M-bit digital display signal (the enhanced resolution provided because M exceeds N). As noted at page 3, lines 29-31 of Applicant's specification, "enhanced digitizer resolution will generate code patterns which easily distinguish between correct and incorrect sampling of analog signals". At page 6, lines 12-15, the specification notes that the task of properly setting a sampler clock "can be effectively accomplished by providing ADCs (42 in FIG. 2) whose conversion resolution substantially exceeds the resolution of the DACs (26 in FIG. 1) that generated the analog display signals".

When the sample clock is properly set, the digital codes of the M-bit digital display signal will be restricted to the 2^N codes that correspond to code counts 88 in Applicant's FIG. 4A. When the sample clock is improperly set, the digital codes of the M-bit digital display signal will be distributed across 2^M codes that correspond to code counts 98 in Applicant's FIG. 4B. It is then a simple matter to adjust the sample clock to limit the observed code counts to those that correspond to the 2^N codes. This is made possible by the enhanced resolution that was provided by quantizing the analog samples to provide the M-bit digital display signal wherein M exceeds N. Without this enhanced resolution, it would not be possible to observe the undesired code counts 98.

In contrast to the processes recited in Applicant's independent claim 1, independent claims 1 and 29 of **Eglit '392** simply recite an analog-to-digital converter "for receiving said analog image data" and state that it uses "a sampling clock to generate a plurality of pixel data elements". Eglit's claims, therefore, fail to address the quantizing process of this converter. In particular, they fail to address the number of bits that the converter provides in its digital display signal. It is noted that the Examiner called attention to claim 8 which is directed to generation of a "multi-bit number --- representative of the amount of phase advance of said sampling clock". This citation concerns the phase of a sampling clock but fails to address the quantizing process of Eglit's converter.

In column 4, lines 53-55 of the specification, it is noted that FIG. 8 is "a block diagram of an example digital display unit in accordance with the present invention" and in column 6, lines 35-36, it is noted that "FIG. 8 is a block diagram of digital display unit 770 including analog-to-digital converter (ADC) 810". Column 6, lines 44-48 then notes that "in operation, the ADC 810 receives analog signal data on line 801 and a sampling clock signal on line 851 --- ADC is conventional and samples the analog signal data according to the sampling clock signal --- ADC 810 provides the pixel data on line 812".

The bulk of the remainder of the specification of Eglit '392 is directed to a "clock recovery circuit 300" (column 4, lines 59-60) which is shown in FIG. 3 to include a digital PLL 310 and an analog filter 320 and to details of these elements which are shown in FIGS. 4, 5 and 6. For example, details of the digital PLL circuit 310 of FIG. 4 are discussed from line 25 of column 7 to line 31 of column 8 and details of the analog filter 320 of FIG. 4 are discussed at lines 43-57 of column 11. An embodiment of the digital PLL circuit is described in considerable detail from line 38 of column 8 to line 50 of column 10. In all of this discussion, however, Eglit '392 fails to address the quantizing process of his converter 810 of FIG. 8. In particular, Eglit '392 mentions an ADC 810 that samples analog signal data and provides pixel data but Eglit '392 never discloses the number of bits to which the analog signal data is quantized.

It is noted that Applicant's claim 1 does not concern the structures of digital PLLs and analog filters but, instead, recites processes that quantize analog samples to provide an M-bit digital display signal wherein M exceeds N and that adjust at least one of the frequency and phase of a sample clock to substantially restrict the codes of the M-bit digital display signal to 2^N different codes

Because Eglit '392 fails to teach the quantizing step of Applicant's claim 1 (and its resulting enhanced resolution) and fails to teach a step of adjusting at least one of the frequency and phase of a sample clock to substantially restrict the codes of an M-bit digital display signal to 2^N different codes, it cannot anticipate Applicant's independent claim 1.

Because Eglit '392 teaches details of digital PLL structures and analog filter structures, it teaches away from Applicant's method as recited in Applicant's claim 1 and cannot therefore contribute to a *prima facie* case of obviousness with respect to this claim.

Applicant's independent claim 1 thus patentably distinguishes over the cited reference. Because claims 2 and 5 add further limitations to claim 1, they also distinguish over the cited reference.

Although the Examiner rejected Applicant's claim 1 over Eglit (5,796,'392), it is noted that Eglit (5,847,701) teaches another conventional method for generating a digital display signal from an analog signal. Because this reference is representative of a number of prior art methods, its teachings are also investigated below.

In contrast to the processes recited in Applicant's independent claim 1, **Eglit '701** "generates a sequence of test patterns comprising a plurality of pixel data elements according to a predetermined convention --- the graphics source converts the pixel data elements into an analog display signal at an original frequency and sends the analog signal to a digital display unit --- (which) samples the analog signal at a sampling frequency to generate a plurality of sampled values" (column 3, lines 10-18). Eglit '701 further notes that a "digital display unit determines whether the sampled values equal a test pattern according to the predetermined convention --- if the sampled values are equal to

the test pattern, the sampling frequency equals the original frequency" (column 3, lines 18-25).

Eglit '701 concludes that the "present invention provides a mechanism by which a display unit can determine the original frequency used by a graphics source to generate an analog display signal --- this feature is provided by encoding the analog display signal with a sequence of test patterns that can be identified by the digital display unit --- if the digital display unit correctly identifies one or more test patterns accurately, the corresponding sampling frequency equals the original frequency" (column 4, lines 11-19).

Eglit '701 shows an exemplary test pattern 920 in his FIG. 9 in which zeros and ones alternate. When the sampling frequency is correct, the test pattern is recovered as shown in the sampled values of the signal 960. When the sampling frequency is less than or greater than the original, incorrect patterns are recovered as shown in the respective sampled values of signals 960 and 990.

Portions of the quotations from Eglit '701 have been underlined above to emphasize that Eglit '701 teaches the insertion of a test pattern into the analog display signal and teaches that a sampling frequency is correct when the test pattern is recovered. It is noted that Applicant's claim 1 method does not recite the use of a test pattern and, instead, quantizes analog samples to provide an M-bit digital display signal wherein M exceeds N

Because Eglit '701 fails to teach this quantizing step (and its resulting enhanced resolution) and fails to teach a step of adjusting at least one of the frequency and phase of a sample clock to substantially restrict the codes of an M-bit digital display signal to 2^N different codes, it cannot anticipate Applicant's independent claim 1.

Because Eglit '701 teaches the insertion of a test pattern, it teaches away from Applicant's method as recited in Applicant's claim 1 and cannot therefore contribute to a *prima facie* case of obviousness with respect to this claim.

Applicant's independent claim 1 thus patentably distinguishes over the cited references. Because claims 2 and 5 add further limitations to claim 1, they also distinguish over the cited references.

It is noted that the amendments of claims 3 and 4 place them in independent form. Because they make no substantive changes in the filed language of these claims, these amendments are unrelated to statutory requirements for patentability and do not, therefore, narrow the scope of the claims.

Applicants therefore request reconsideration and withdrawal of the rejections and an early allowance of claims 1-5 to thereby join already-allowed claims 6-13.

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